REMARKS

Claims 1-18 are currently active.

Antecedent support for the amendments to the claims is found on page 7, lines 4-10.

Sakamoto does not teach or suggest "counting the data that has been received, transmitted or dropped by the primary component and the secondary component of the switch after a switchover event occurs without including any redundancy in the counting of the data due to the primary component and secondary component both able to switch data through the switch".

Referring to Sakamoto, there is disclosed an ATM handler. Sakamoto teaches in a control system in which the control part 4 issues a system switchover order of a particular path via the control line 6 to the selector card 3 and in order of count operation change-over independently to a pair of line interface cards 1-1 and 1-2 corresponding to the switchover path, there appears a difference in time between the values of arrival time of the order to the respective cards, the difference being decided by the communication protocol. Resultantly, between the system switchover time by the selector and the change-over time of count

operation by the pertinent line interface circuits, their occurs a delay in time which cannot be disregarded. See column 8, lines 41-52.

Sakamoto teaches to solve the problem above according to their invention, the control part 4 issues the system switchover order only to the selector card 3. In response to the order, the status value of the selector control register 27 on the selector card 3 is altered such that the selector 9 switches over the system in response to a system switchover signal output from the register 27. Between the line interface cards 1 and the selector card 3, the signal line 26 is individually installed for each pair of line interface circuits 15 such that the system switchover signal is supplied via the individual signal line 26 to each line interface circuit 15 to thereby synchronize the system switchover by the selector 9 with the change-over of count operation of user cells by each line interface circuit 15.

Sakamoto teaches that figure 10 schematically shows the relationship between streams of cells 51-0 and 51-1 respectively inputed to the line interface circuits 15-1 and 15-2 respectively of the working and protection paths, operation to count cells (indicated by an asterisk), and a stream of cells 51-2 from the selector line. It is assumed, that the abscissa represents the lapse of time and the phase difference is missing between the streams of input cells respectively of the working and protection paths. In a case where the selector switches over the system as a point of time 52 when the line interface circuit 15-1 of the working path

in the active status counts the fifth input cell 50, a line interface circuit 15-2 of the protection path interrupts the cell counting operation substantially at the same time. Thereafter, the line interface circuit 15-2 of the protection path thus set as the active system commences the cell accounting operation. See column 9, lines 51-67.

Sakamoto teaches that as it can be understood from cell numbers of cells indicated by an asterisk, the line interface circuit 15-2 of the protection path starts accounting operation beginning at a cell 50' (sixth cell) next to the last cell 50 (fifth cell) counted by the line interface circuit 15-1 of the working path. Moreover, since the stream of cells output from the selector 9 matches the cells counted on the input side, the line interface circuit on the output side can correctly count cells. See column 10, lines 1-9. As is clearly evident from this description, Sakamoto teaches that cells just continue sequentially but at some point simply divert to an alternative circuit. There is no contemplation, consideration or thought that cells could be lost or duplicated in the teachings of Sakamoto.

Sakamoto further teaches that when the control part 4 issues a system switchover order 93 to the selector card 3, the setting value of the selector control register 27 is changed over and hence the signal status of the wire 26 is varied. The status change of the wire 26 is notified as a system switchover signal line for the switchover the selector 9. Simultaneously, the hardware system for working path (15-1 of the line interface circuit 1-1)

stops the cell counting operation 95 and then the hardware system for protection path to be set as the active system 50 (15-2 of the line interface circuit 1-2) hence commences counting cells 96. See column 10, lines 57-67.

Sakamoto does not teach or suggest to count and compensate for both the primary and secondary components of the switch, let alone after a switchover event occurs. Sakamoto does not even consider the possibility that cells could be dropped or duplicated in regard to the switchover event. Figure 10 of Sakamoto teaches that Sakamoto only considers a switchover without any loss or duplication of cells. Thus, Sakamoto teaches away from the claimed invention because Sakamoto teaches loss or duplication cannot occur. This follows because as explained above, Sakamoto is concerned with the problem that when a switchover occurs, there is a delay in time of the count operation by the pertinent line interface circuit, which cannot be disregarded. See column 8, lines 49-53 of Sakamoto. Accordingly, applicant's claimed invention, as amended, is patentable over Sakamoto.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-18, now in this application be allowed.

CERTIFICATE OF MAILING

I hereby certify that the correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

on 6/15/04

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